Claims

1. A comparator circuit with controlled outer transistor stage bias currents, comprising:

an outer transistor stage, including:

a first transistor including a signal input terminal, a first output terminal and a second output terminal; and

a second transistor including a reference input terminal, a first output terminal and a second output terminal, wherein the first and second output terminals of the first and second transistors are coupled across a power source, and wherein the first and second transistors of the outer transistor stage provide drive currents to transistors of an inner transistor stage; and

bias current control circuitry for controlling bias currents associated with the first and second transistors, wherein the bias current control circuitry minimizes the bias currents when a magnitude of an input signal at the signal input terminal is a predetermined value from a magnitude of a reference signal applied to the reference input terminal, and wherein the bias current control circuitry increases the bias currents associated with the comparator circuit when the magnitude of the input signal at the signal input terminal is within the predetermined value of the magnitude of the reference signal at the reference input terminal.

2. The comparator circuit of claim 1, wherein the input and reference signals are voltage signals.

3. The comparator circuit of claim 1, wherein the bias currents are increased when the magnitude of the input signal at the signal input terminal is within the predetermined value of the magnitude of the reference signal at the reference input terminal.

4. The comparator circuit of claim 1, wherein the bias currents are at a desired magnitude when the magnitudes of the input and reference signals are substantially equal.

5. The comparator circuit of claim 1, wherein the signal input terminal is a non-inverting input and the reference input terminal is an inverting input.

6. The comparator circuit of claim 1, wherein the predetermined value is about 50mV.

7. The comparator circuit of claim 1, wherein the transistors are bipolar transistors.

8. The comparator circuit of claim 1, further including:

a blinding timer discharge current source configured to limit current drawn by the blinding timer discharge current source while a capacitor coupled to the input signal terminal is being charged, wherein the blinding timer discharge current source is coupled across the capacitor.

9. The comparator circuit of claim 1, wherein the signal input terminal includes an associated leakage current compensation circuit.

10. A method for reducing input currents associated with a comparator circuit during certain events, comprising the steps of:

minimizing bias currents associated with a comparator circuit when a magnitude of an input signal at a signal input of the comparator circuit is a predetermined value from a magnitude of a reference signal applied to a reference input of the comparator circuit; and

increasing the bias currents associated with the comparator circuit when the magnitude of the input signal at the signal input of the

comparator circuit is within the predetermined value of the magnitude of the reference signal at the reference input of the comparator circuit.

11. The method of claim 10, wherein the bias currents are applied to outer stage transistors of the comparator circuit.

12. The method of claim 10, wherein the input and reference signals are voltage signals.

13. The method of claim 10, wherein the bias currents are increased when the magnitude of the input signal at the signal input of the comparator circuit is within the predetermined value of the magnitude of the reference signal at the reference input of the comparator circuit.

14. The method of claim 10, wherein the bias currents are at a desired magnitude when the magnitudes of the input and reference signals are substantially equal.

15. The method of claim 10, wherein the signal input is a non-inverting input and the reference input is an inverting input.

16. The method of claim 10, wherein the predetermined value is about 50mV.

17. An automotive ignition system including a comparator circuit with controlled outer transistor stage bias currents, the comparator circuit comprising:

an outer transistor stage, including:

a first transistor including a signal input terminal, a first output terminal and a second output terminal; and

a second transistor including a reference input terminal, a first output terminal and a second output terminal, wherein the first and

second output terminals of the first and second transistors are coupled across a power source, and wherein the first and second transistors of the outer transistor stage provide drive currents to transistors of an inner transistor stage; and

bias current control circuitry for controlling bias currents associated with the first and second transistors, wherein the bias current control circuitry minimizes the bias currents when a magnitude of an input signal at the signal input terminal is a predetermined value from a magnitude of a reference signal applied to the reference input terminal, and wherein the bias current control circuitry increases the bias currents associated with the comparator circuit when the magnitude of the input signal at the signal input terminal is within the predetermined value of the magnitude of the reference signal at the reference input terminal, where the bias currents are at a desired magnitude when the magnitudes of the input and reference signals are substantially equal.

18. The system of claim 17, wherein the signal input terminal is a non-inverting input and the reference input terminal is an inverting input.

19. The system of claim 17, further including:

a capacitor coupled across the signal input terminal of the first transistor and a signal return line; and

a blinding timer discharge current source coupled to the signal input terminal of the first transistor, wherein the discharge current source is configured to reduce an associated current to substantially its leakage current when the current source is off.

20. The system of claim 19, further including:

a switch coupled across the capacitor, wherein the switch is configured to reduce an associated current to substantially its leakage current when the switch is off .